

# Dendritic Computation: Routing Neuroscience to Neuromorphic Circuits

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## **Primary Theme: Neuroscience algorithms and translation to neuromorphic analog circuits**

### Neuroscience-inspired computing principles

Neuroscience insights have long informed and inspired the design of neuromorphic systems [1]. This interdisciplinary approach has enabled the development of novel computing technologies but also holds promise to advance our understanding of the brain. However, while the neuroscience field continues to grow with tremendous explosion of new data, the neuromorphic field is still lagging in its translation. For example, the fundamental computational unit in a brain is the neuron. A single neuron is quite complex in biology across species from invertebrates to mammals. The structure of dendrites within a neuron are often quite intricate, vary widely and depend on the neuron's specific sub-type and location within a brain, and can be specialized to support the function of the neuron [2,3,4]. However, modern neuromorphic and artificial neural networks adopt a much simpler and homogeneous model of the neuron leading to increased reliance on scaling. Our hypothesis is that thoughtful consideration of the complexity and heterogeneity of a single neuron (specifically with dendrites) can lead to the design of smaller systems with increased computational complexity.

### Translation to analog microelectronic circuits

Modeling dendrites in analog circuits is crucial to getting the computational density (operations/unit) as well as computational efficiency (energy/operations/second). Dendrites within a neuron can be thought of as a "neural network within a single neuron" [5] enabling compute-on-wire. Current architectures focus solely scaling number of neurons and synapses per neuron. Most emerging non-volatile devices can be used to construct dendrites offering a "dendritic toolkit" which include non-linear filtering, spatio-temporal processing, gain modulation, coincidence detection while offering dense connectivity [6,7,8]. In prior work, we have demonstrated the efficacy of analog dendrites using the following circuits:

- 1) Direction-Selective Dendrite Circuits (Pattern Recognition [9], Near-sensor processing [9]), Dragonfly TSDNs (Target Selective Descending Neurons)[10], Fruit Fly Visual ON Circuit[11])
- 2) Dendrites for Gain modulation (Dragonfly Coordinate Transformation for Interception [9])
- 3) SNNs with Dendrites (Coincidence Detection[12], Non-linear functions[12], Pooling layers[11]).

These circuit motifs can be used to demonstrate large-scale dendrite-based neural networks. Emerging devices as well as novel approaches in fabrication like 3D architectures, wafer-scale technology, and in-memory computing could further alleviate current communication and connectivity bottlenecks.

### Modeling and simulation approaches

Existing neural simulators such as NEURON, BRIAN 2, and NEST can be used to model large-scale SNNs. To incorporate dendrites in SNNs, we can use Dendripy as well as our own dendrite library that models hardware-based parameters for snnTorch [12]. We have also developed a neuromorphic architecture simulator called SANA-FE [13] with plans to incorporate multiple emerging hardware-based dendrites and enable design space exploration of novel dendrite-based architectures.

### Performance metrics, data requirements, and energy efficiency

Dendrites can be evaluated based on performance (operations/second) as well as energy efficiency (energy/operation/second). Other metrics include accuracy, latency, area, and ease-of-integration. Ideally, analog datasets should be created (much like event camera datasets) for evaluation and benchmarking various hardware-based approaches.

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