Platform Readiness
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Software Products

OpenACC+OpenMP / OpenARC
- Open-sourced, OpenACC/OpenMP compiler supporting NVIDIA/AMD GPUs, Intel Xeon Phis, and Altera FPGAs.
- [https://ft.ornl.gov/research/openarc](https://ft.ornl.gov/research/openarc)
- Contact: Seyong Lee, lees2@ornl.gov

OpenACC on LLVM / Clacc
- CLACC: OpenACC support for Clang/LLVM
- Automated translation from OpenACC source to OpenMP source.
- [https://ft.ornl.gov/research/clacc](https://ft.ornl.gov/research/clacc)
- Contact: Seyong Lee, lees2@ornl.gov

Deep Memory Hierarchies
- Papyrus: a novel programming system for aggregate distributed NVMs.
- [https://ft.ornl.gov/research/papyrus](https://ft.ornl.gov/research/papyrus)
- AML: building blocks for deep-memory aware algorithms.
- [https://xqitlab.cels.anl.gov/argo/aml](https://xqitlab.cels.anl.gov/argo/aml)

Code Generation and Autotuning
- Compiler optimization of sparse matrix computations
- Autotuning of OpenMP or OpenACC pragmas underway
- [https://github.com/CtcpSltahEdu/chill.git](https://github.com/CtcpSltahEdu/chill.git)

Roofline Modeling
- Model for identifying performance bottlenecks in applications
- Applied to CPUs/KNL/GPUs
- [http://crd.lbl.gov/roofline](http://crd.lbl.gov/roofline)
- Contact: Sam Williams (SWWilliams@lbl.gov)

Application Engagement

- Outreach to ScIDAC and other applications teams for assessment of their platform readiness challenges.
- Present tutorials and hackathons.
- Coordinate with the AE on tiger teams.

Hierarchical Roofline in Advisor
- RAPIDS/NERSC/Intel developed & analyzed cache-simulator Roofline
- Integrated into Intel Advisor.
- Measures data movement through cache hierarchy & identifies bottlenecks.

MPI Message Reordering
- Reordering messages improves performance.
- Applicable to MPI/GASNet, Aries/InfiniBand
- 1.7x on HPGMG, 1.2x on FFTs, 1.2x on Sort

Roofline on CPU/KNL/GPUs
- CRD/NERSC/LANL developed perf. counter Roofline methodology
- Applied to GPP and AMReX proxies.
- Low overhead analysis of MPI+ OMP/CUDA apps.

KORC: Kinetic Orbit Runaway Code
- Performed initial assessment and identified/optimized redundant computations.
- Designed a basic GPU porting strategy using OpenACC/OpenMP.

Focus Areas:

- Preparing applications for current and upcoming architectures through best-in-class expertise and tools.
- Portable programming for heterogeneous and many-core systems, deep memory hierarchies
- Code generation and autotuning for computation and communication
- Performance modeling and analysis for identifying optimization opportunities
- Correctness of programs (e.g., when moving to new platforms)
- Tools: CHILL, CIVL, various compilers (ROSE, OpenARC, LLVM), Roofline toolkit, Orio, Papyrus, SCR, TAU

Program Correctness (CIVL)
- Formal verification of parallel programs to verify equivalence of two implementations or verifying safety properties (e.g., deadlock-free)
- C and Fortran + MPI, OpenMP, and/or CUDA
- [http://vsl.cis.udel.edu/civl, siegel@udel.edu](http://vsl.cis.udel.edu/civl, siegel@udel.edu)

TAU Performance System®
- Profile, trace, and sampling measurement, analysis, and visualization toolkit
- MPI, OpenMP, OpenACC, Python, CUDA, PAPI
- [http://tau.oregon.edu](http://tau.oregon.edu)
- Contact: Kevin Huck (khuck@cs.uoregon.edu)

Motivation
ASCe Computing Systems are growing more complex with
- heterogeneous compute and
- deep memory hierarchies, and
- ambiguous, non-portable programming models and libraries.

Publications