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Data Acquisition Systems

Design and Fabrication of the ASoC: Analog to digital converter System on a Chip

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Aug 13, 2019

DOE Phase II SBIR Exchange Meeting

Grant: DE-SC0015231- SBIR Phase II, Year 2: 4/9/2017-4/8/2019, NCE until 11/30/2019

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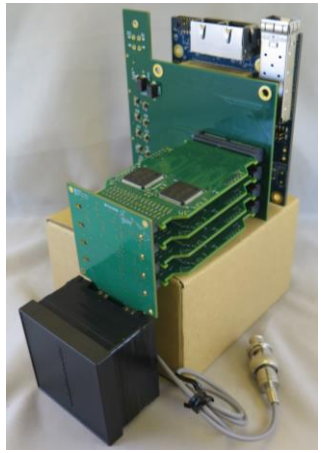
Waveform Digitizer SoCs for Single Photon Time of Flight Detection: Compact, Low Cost, Low Power

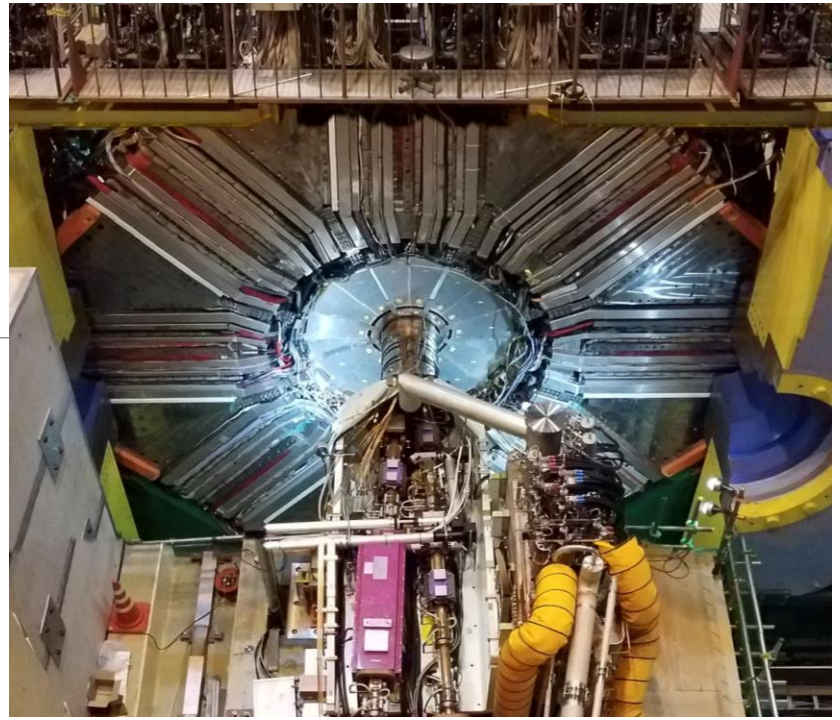
1. Various Front-end Chips:

- Event based digitizer+DSP
- 4-32 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP
- Low cost
- User friendly



2. Integration:

- SiPM
- PMT
- LAPPD
- Antenna arrays



3a. Main application: Particle collider experiments (Belle II at KEK in Japan)

3b. Other applications:

- Beam diagnostics
- Plasma /fusion diagnostics
- Lidar
- PET imaging

About Nalu Scientific

Nalu Scientific
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Integrated Circuits Design

- Analog + digital System-on-Chip (SoC)
- Digital implementation

Hardware Design

- Field Programmable Gate Arrays (FPGA)
- Complex multi-layer Printed Circuit Board (PCBs)

Expertise in:

- Time of Flight (ToF) measurements
- Fast timing
- Radiation detection
- Readout electronics for Particle Physics

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Team

Isar M.
Founder and CEO
UH PhD EE
3x Entrepreneur

Luca M.
Senior Engineer
PhD EE, 20+ yrs
IC Design Lead

Dean U.
Senior Engineer
30+ yrs experience
Digital IC Design

Ryan P.
Senior RF Engineer
10+ yrs experience
High Frequency Design

Ben R.
Staff Physicist
PhD Phys
Particle Physics Guru

Chris C.
Design Engineer
BS CE
Agile R&D

Angela A.
Office Manager
Admin Guru

Marcus L.
SW/PM

Kenneth L.
EE

Advisors

Shawn U.
Gov. Relations

Ryan O.
Media Relations

Prof. Gary V.
UH Subcontract

+ University of Hawaii team:

3 Postdocs

3 PhD candidates at University of Hawaii

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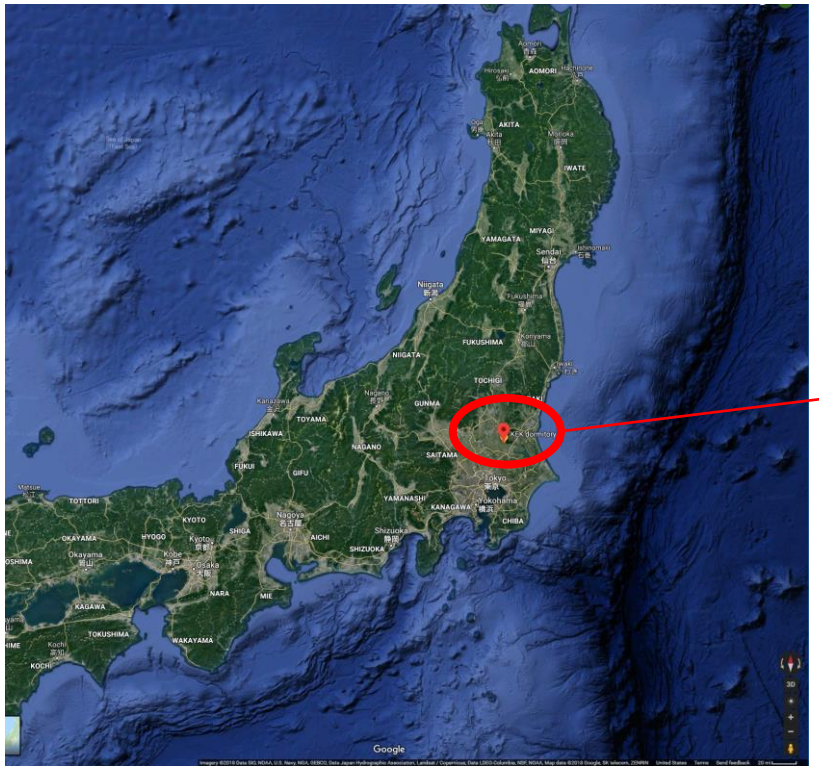
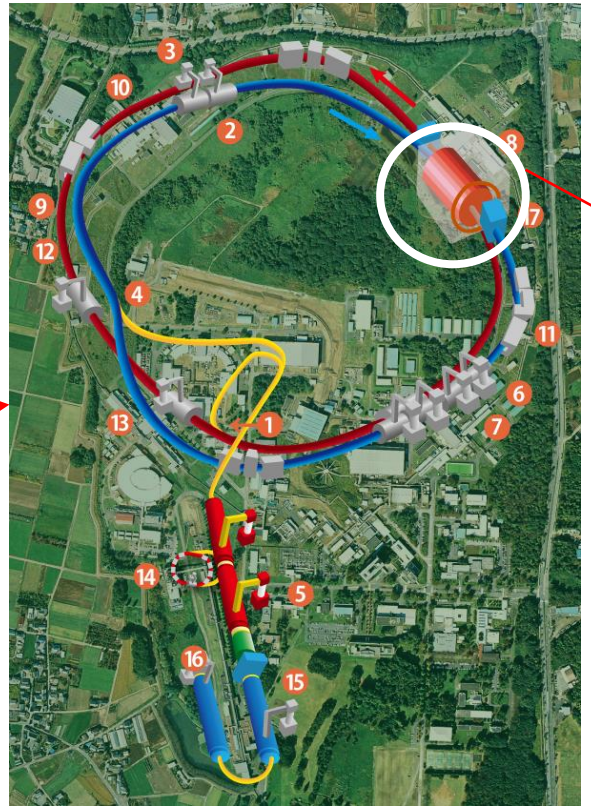
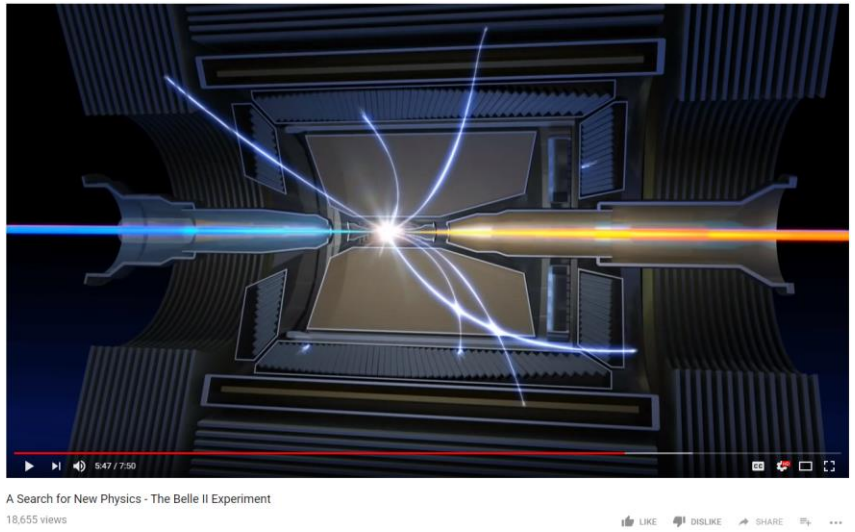
Where did we start?
A Search for New Physics – The Belle II Experiment



Tsubuka City
Located 60 mi north of Tokyo



High Energy Accelerator Research Facility (KEK) in Tsukuba



Interaction point inside the electron/positron collider

Some History:

Belle II Upgrade is a 26 Country, 900+ member Collaboration

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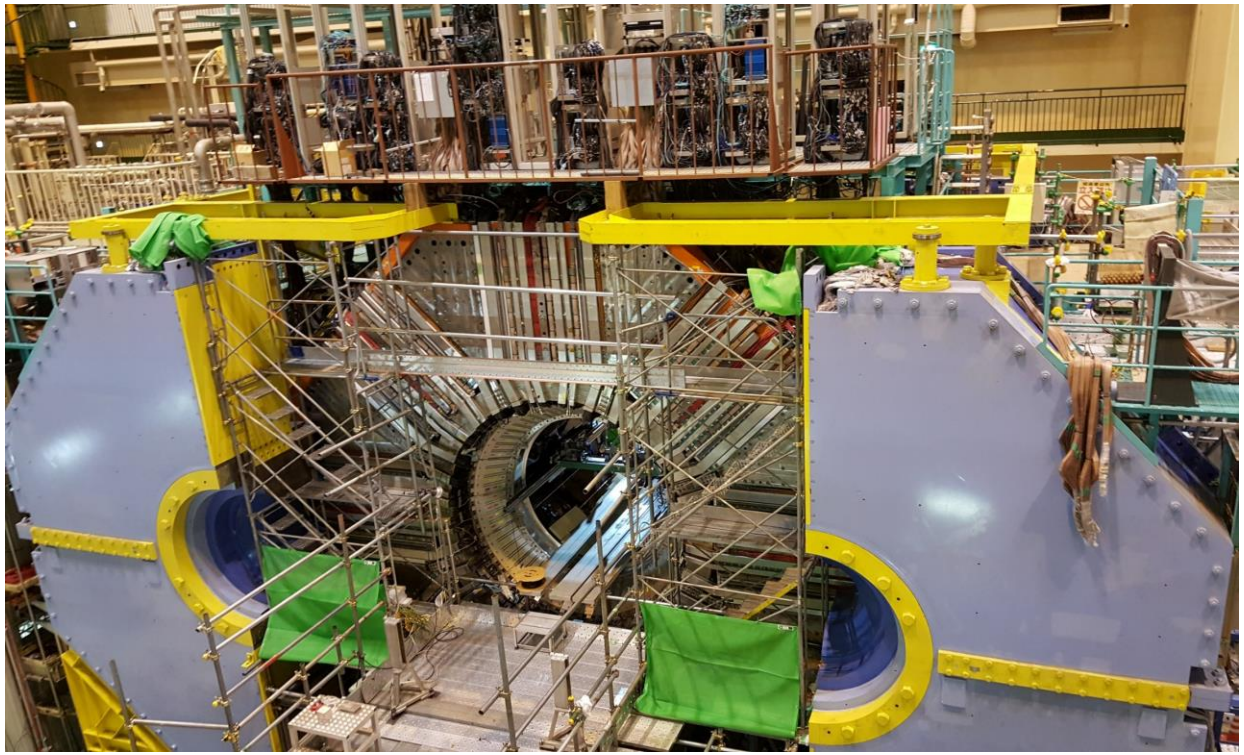
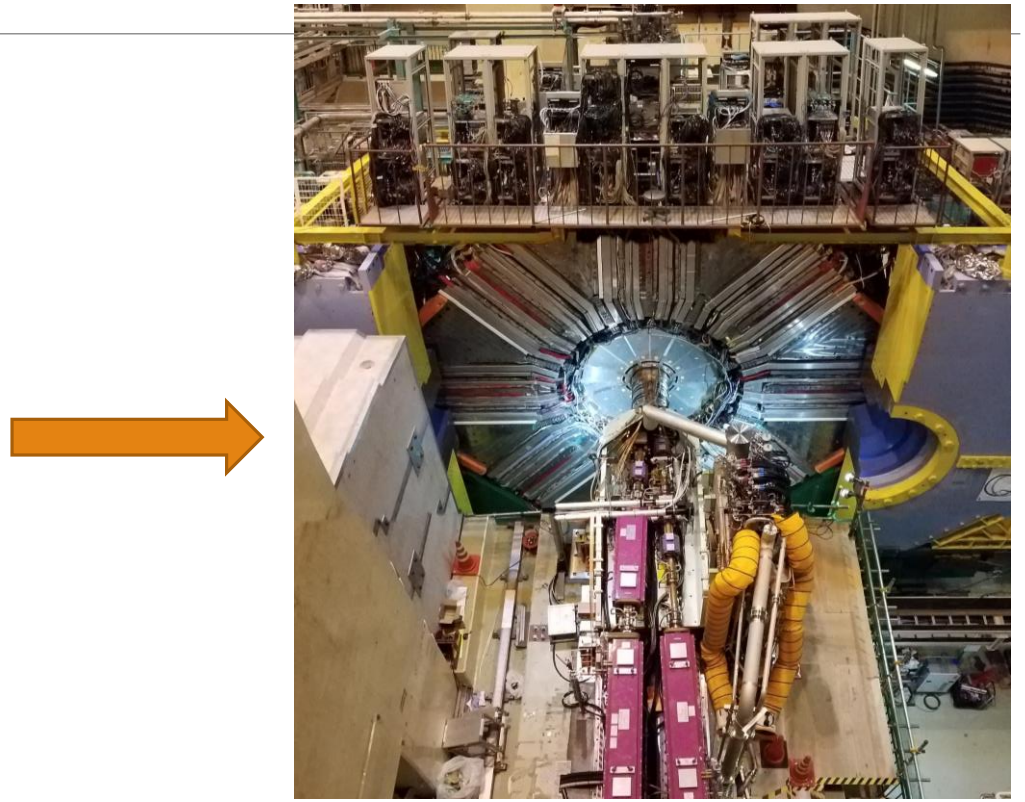
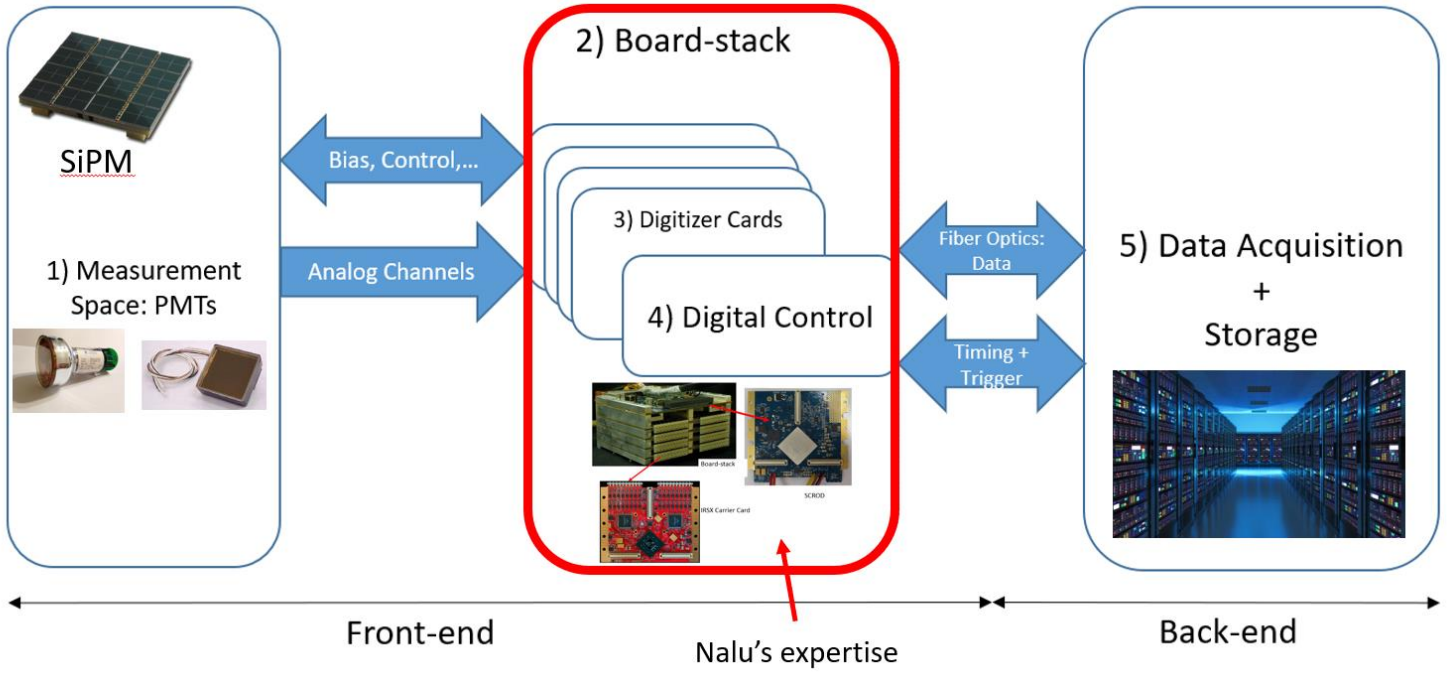




2015 **2018**

Belle II: e+ e- experiment at 40x luminosity of Belle -> Detector needs to operate at severe beam background

Lesson 1:
How does a Particle Physics Experiment Work?



Lesson 2:
Opportunities

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Next gen Particle Physics electronics need to be:

- Radiation hard
- High performance
- Low cost, low power
- And **user friendly**

Solution: New System-on-Chip Integrated Circuit Design

Opportunity: Not many commercial options available

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Benefits of Higher Integration - SoC

- **Analog memory:**
  - Sampling always on (1-10 Gsa/s), but at low power
  - Digitize only Region of Interest (ROI)
  - Long analog buffer -> suitable for large experiments
- **Digital processing:**
  - Per channel cost reduction by a factor of 4
  - Relax thermal design by 40% reduction in power dissipation
  - Trigger time-stamping at the front-end
  - Eliminating the need for costly high-end FPGAs
  - User friendly: substantially reducing the FPGA firmware development labor
  - Reduced complexity and design and cabling effort/cost for the front-end boards

Analog/Mixed signal design

+

Digital/Synthesized logic

=

System-on-Chip (SoC)

Nalu Scientific SBIR Project: ASoC

Compact, high performance waveform digitizer

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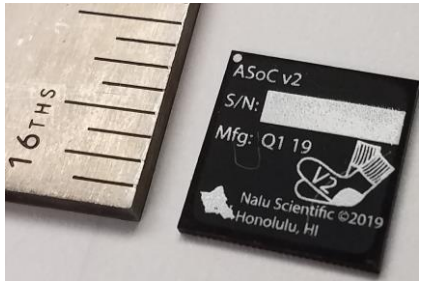
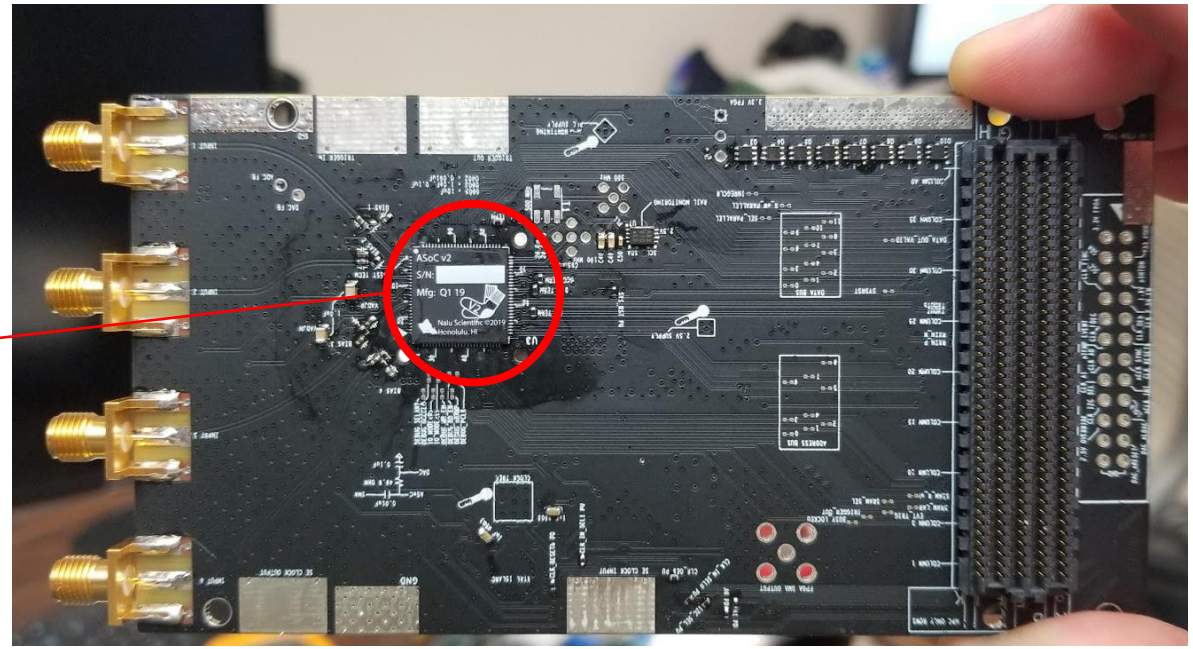
Parameter	Spec (measured)
Sample rate	2.4-3.2GSa/s
Number of Channels	4
Sampling Depth	16kSa/channel
Signal Range	0-2.5V
Resolution	12 bits*
Supply Voltage	2.5V
RMS noise	~1 mV
Digital Clock frequency	25MHz
Timing resolution	<25ps**
Power	140mW/channel
Analog Bandwidth	950MHz





Key Contribution:

- High performance digitizer: 3+ Gsa/s
- Highly integrated
- Commercially available
- 5mm x 5mm die size

Chip fabricated in 250nm CMOS
Very low cost to prototype and mass produce

All chips, are designed with commercial grade tools and licenses and can be sold once commercialized.

ASoC V2 Measurements

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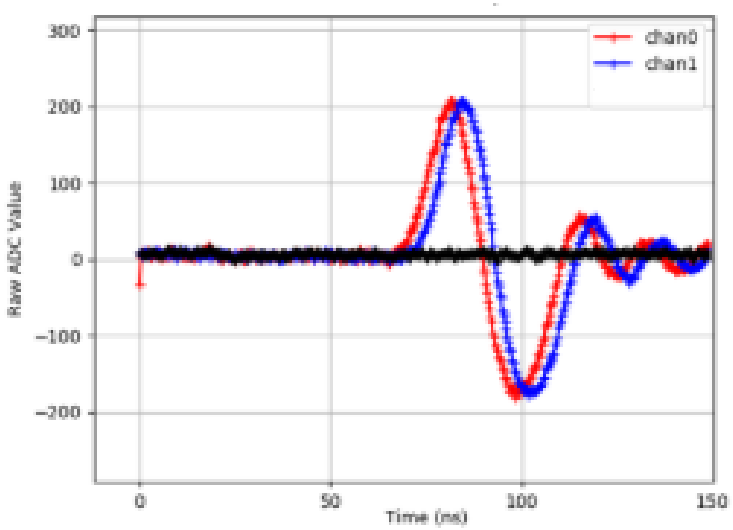
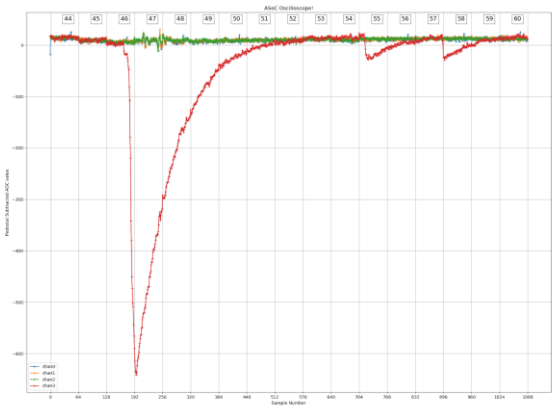
Live demo at IEEE NSS-MIC 2018



SiPM waveform readout



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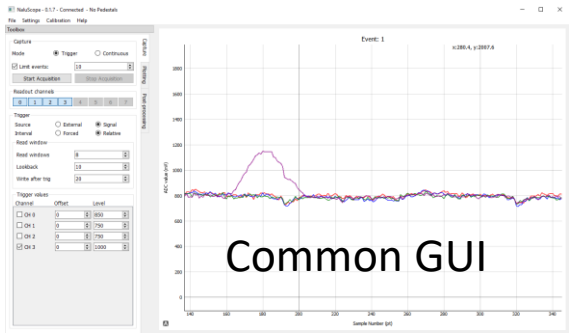
ASoC Phase II - Schedule

1. 3x ASoC revisions proposed
2. 2x fabricated, 1x planned for October 2019
   - ASoC eval cards currently under test by collaborators (Labs, companies)
3. In each revision more components are qualified and tested on Silicon:
   - High frequency Phased Locked Loops (PLLs) – Clock gen
   - High speed serial comm
   - Various amplifiers and switches
4. Moving from function to performance:
   - Identify and reduce non-idealities: Noise, non-linearity, temperature variations
   - On chip calibration, reduce deadtime, data reduction and packaging
5. Beyond Phase II:
   - ASoC works well in lab, but needs more robustness for real world
   - Board level integration
   - Firmware, software, GUI



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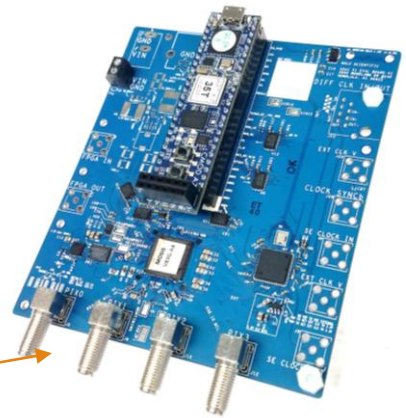
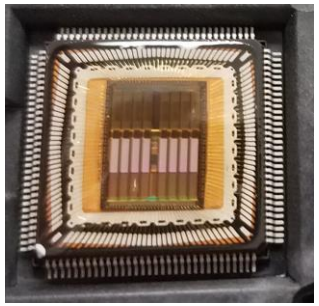
Current SoC-ASIC Projects

Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Available Date
ASoC	3-5	0.8	32k	8	35	Rev 2 avail
SiREAD	1-3	0.6	4k	64	80-120	Rev 1 avail
AARDVARC	6-10	2.5	32k	4-8	4-8	Rev 2 avail
AODS	1-2	1	8k	1-4	100-200	Nov 2019



- **ASoC**: Analog to digital converter System-on-Chip
- **SiREAD**: SiPM specialized readout chip with bias and control
- **AARDVARC**: Variable rate readout chip for fast timing and low deadtime
- **AODS:** Low density digitizer with High Dynamic Range (HDR) option



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Synergies:

Using AARDVARC V2 for measuring PLL output of ASoC V2

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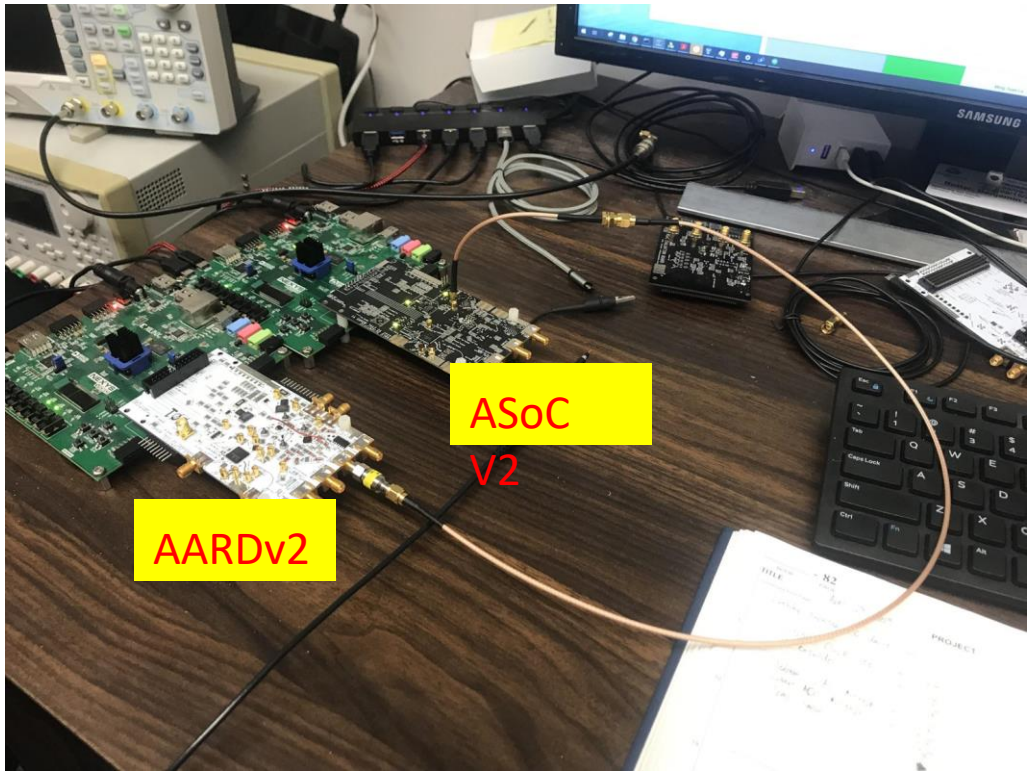
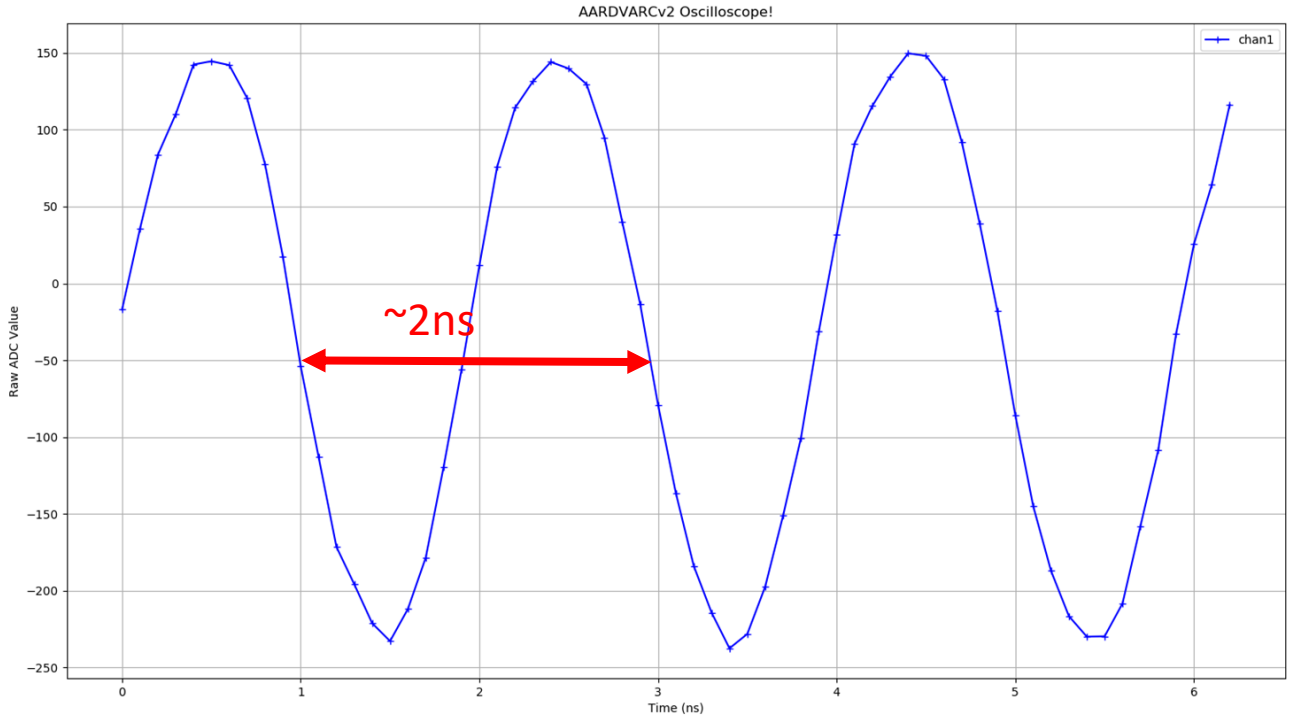


500MHz PLL Output from ASoC V2



Synergies: LAPPD

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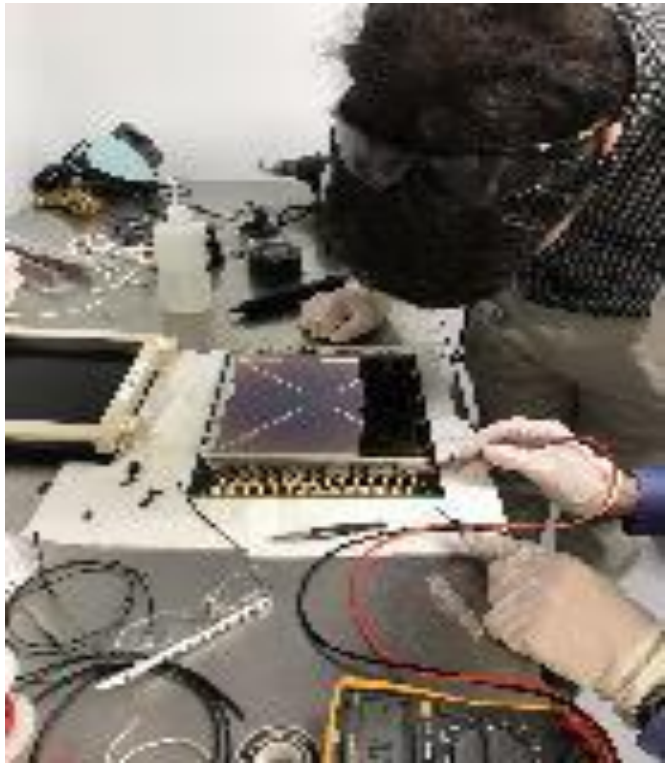
In June 2019 we measured LAPPD pulses using ASoC and AARDVARC chips. We are still analyzing the data.



Synergies: MaPMT Readout for EIC R&D

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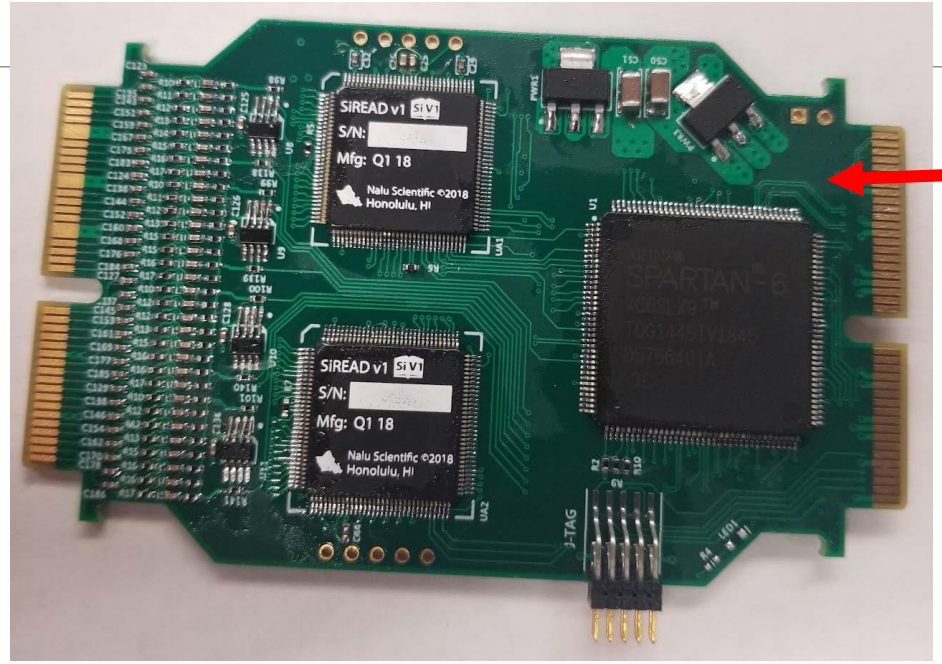
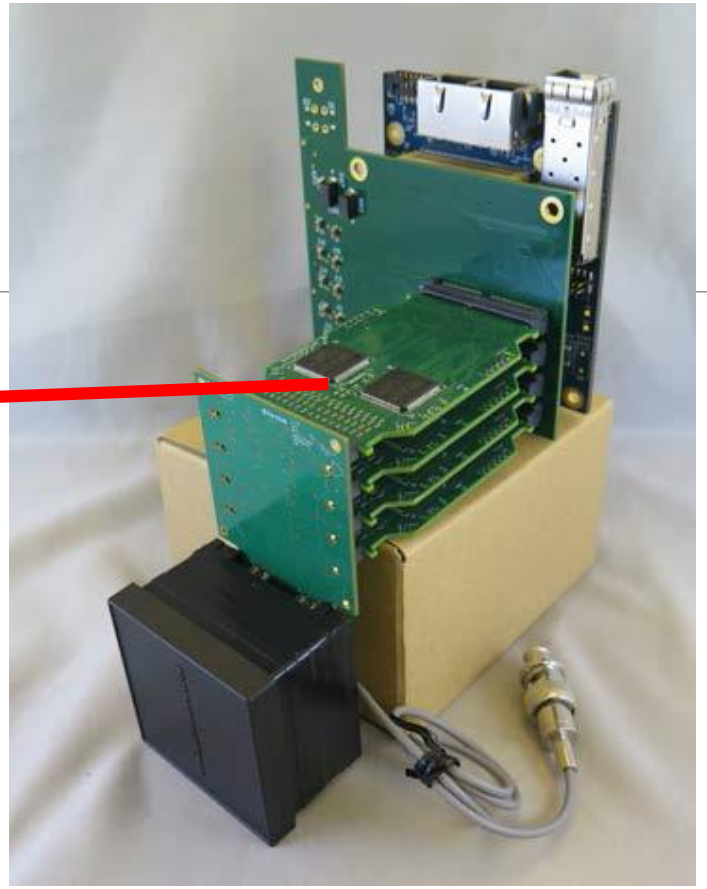
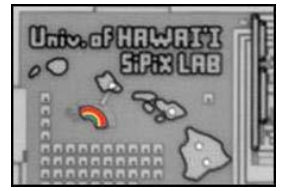


Photograph of the 64 channel SiREAD based (2x SiREAD rev.1) readout card as a building block for the 256 MA-PMT readout.



Photograph of the first generation of 256-anode 2" PMT readout for use with mRICH prototype in the Fermilab beam test facility.



In the news and events

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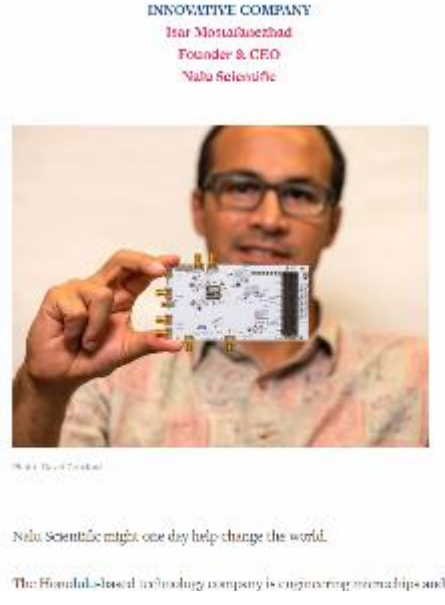
Pacific Biz News 40 under 40

Booth and AARDVARC Live demo at US-Japan Particle Physics Symposium in Honolulu (April 2019)

Next Top Startup Pitch Competition
Runner up - IMS2019 - Boston



Hawaii Biz Magazine
Most Innovative Small Biz of the year

IEEE Young Professionals Panel
IMS2019 - Boston

IPAC 2019 booth- Melbourne

Hawaii Congressman Ed Case visit

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Acknowledgements

US Department of Energy Office of Science

Hawaii Technology Development Corporation (HTDC)

University of Hawaii Department of Physics