Performance Portability and Programming Models for C++ codes

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New Machines Coming! Look busy!





- AMD CPU + NVIDIA GPU
- Cray Slingshot Interconnect

If your code runs well on current NVidia GPUs using CUDA Or OpenACC you should be Well positioned for Perlmutter



Intel CPU + Xe Technology



- AMD CPU + AMD GPU
- ROCm (HIP)

If your code runs well on Summit with CUDA, Converting to HIP may be mostly automated



What are some options out there?

OpenMP & OpenACC

Kokkos & Raja





- #pragma directives for
 - Parallel for
 - Reduction
 - SIMD
 - Offload
 - Tasking
- Relies heavily on compiler

- More C++ oriented
 - Modern C++
 - Parallelism via functors & lambdas (forall, ...)
 - Policy driven (execution & memory spaces)
- Many back ends - OpenMP, CUDA, ROCm,...







OpenMP

- Offloaded axpy in OpenMP
 #pragma omp target teams distribute parallel for simd
 map(to:z[:N]) map(a,x[:N],y[:N])
 for(int i=0; i < N; i++) // N is large
 {
 z[i] = a*x[i] + b[i];
 }
 </pre>
 - Collapses:
 - omp target target the accelerator,
 - omp teams create a league of teams
 - omp distribute distribute the works amongst the teams
 - omp parallel for simd perform a SIMD-ized parallel for
 - map a, x and y to the accelerator and map resulting z back out.





Kokkos

Kokkos::View<float[N],LayoutLeft,CudaSpace> x("x"); // N is large Kokkos::View<float[N],LayoutLeft,CudaSpace> y("y"); Kokkos::View<float[N],LayoutLeft,CudaSpace> z("z");

float a=0.5;

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Kokkos::parallel for("zaxpy", N, KOKKOS LAMBDA (const int& i) { z(i) = a*x(i) + y(i); // view provides indexing operator() });

- View multi-dimensional array, index order specified by Layout, location by MemorySpace policy. Layout allows appropriate memory access for CPU/GPU
- Parallel for dispatches a C++ lambda
- **Portable:** Parallel for done with back end: OpenMP, CUDA, ROCm, ...
- Kokkos developers on C++ standards committee work to fold features into C++



Kokkos Performance Summary

Lattice QCD Wilson Dslash Operator (Sparse MV) *Vol=32x32x32x32 sites*













Kokkos Performance Summary

Lattice QCD Wilson Dslash Operator (Sparse MV)









Vol=32x32x32x32 sites





HIP

- HIP is AMD's "C++ Heterogeneous-Compute Interface for Portability"
- Take your CUDA API and replace 'cuda' with 'hip':
 - cudaMemcpy() -> hipMemcpy()
 - kernel<<>>() -> hipLaunchKernel(kernel,...)
 - and other slight changes.
 - You can use *hipify* tool to do first pass of conversion automatically
- Open Source
- Portability between NVIDIA and AMD GPUs only.











SyCL

- C++11 based standard by Khronos group.
- Follows concepts of OpenCL
 - buffers, command queues, kernels, etc
- 'Single Source File' compilation
 - OpenCL kernels were in separate files
- much less verbose than OpenCL

Queue myQueue;

float a = 0.5;{

}); });







```
buffer<float,1> x buf(LARGE N);
buffer<float,1> y buf(LARGE N);
buffer<float,1> z buf(LARGE N);
// ... fill buffers somehow ...
myQueue.submit([&](handler& cgh) {
  auto x=x buf.getAccess<access::mode::read>(cgh);
```

```
auto y=y buf.getAccess<access::mode::read>(cgh);
```

```
auto z=z buf.getAccess<access::mode::write>(cgh);
```

```
cgh.parallel_for<class zaxpy>(LARGE_N,[=](id<1> id){
    auto i = id[0];
    z[i]=a*x[i] + y[i];
```





SyCL

- SYCL manages buffers
- Only access buffers via accessors
- can track accessor use and build data dependency graph to automate data movement
- What does this mean for non SyCL Libraries with pointers? (e.g. MPI)

```
Queue myQueue
buffer<float
buffer<float
buffer<float
```

```
// ... fill bug
float a = 0.9
{
```

```
myQueue.submit
auto x=x_bu
auto y=y_bu
auto z=z_bu
```

```
cgh.paralle
auto i
z[i]=a?
});
});
```







<pre>>; ,1> x_buf(LARGE_N); ,1> y_buf(LARGE_N);</pre>	SyCL runtime manages data in buffers
<pre>,1> z_buf(LARGE_N);</pre>	access buffer data via accessors in
ffers somehow 5;	command group (cgh) scope or host
it([&](handler& cgh) {	accessor
<pre>if.getAccess<access::mode::read>(cgh); if.getAccess<access::mode::read>(cgh);</access::mode::read></access::mode::read></pre>	
<pre>if.getAccess<:mode::write>(cgh);</pre>	
<pre>el_for<class zaxpy="">(LARGE_N,[=](id<1> id){</class></pre>	
<pre>*x[i] + y[i]; kernels mu unique nar</pre>	ust have a ne in C++





How is SyCL portable?

- Essentially SyCL compiler creates **OpenCL** kernels from the Command Group Kernel functors/lambdas
- These can (in principle) compile into
 - SPIR: The Khronos Group's 'Standard Portable Intermediate Representation'
 - PTX: for NVIDIA GPUs
 - HIP and/or GCN ISA for AMD
- The final result can be consumed by the target machine runtime.
- Many SyCL implementations are available











Summary

- Lots of options: OpenMP, Kokkos, RAJA, SyCL, HIP etc.
 - but will there be one that works well on all of Perlmutter, Aurora and Frontier?
- There are similarities, with differences between Kokkos, Raja, and SyCL
 - Express parallelism via functors/lambdas
 - Data Movement: Views v.s. Buffers, Explicit v.s. Implicit movement, Accessor Scope.
- Parallel features are also being incorporated into standard C++
 - parallel algorithms, pSTL, std::simd, etc...
 - Kokkos developers & others are members on the C++ standards committee
- I have had some very positive experiences with Kokkos
 - Performance was within 20% or so of hand tuned code on P100 (SummitDev) even better on Volta.
 - Performance matched hand tuned code on KNL after manual vectorization of complex. Kokkos::simd will fix this(?)
- Need to repeat these experiments with OpenMP & SyCL
 - ongoing current work. I hope to have more results on this soon.
 - as always: your application's mileage may vary.









References

- OpenMP: <u>https://www.openmp.org/</u>
- Kokkos: <u>https://github.com/kokkos/kokkos</u>
- RAJA: <u>https://github.com/LLNL/RAJA</u>
- SyCL: <u>https://www.khronos.org/sycl/</u>
- Intel One API
- Performance Portability: <u>https://performanceportability.org/</u>







HIP: <u>https://gpuopen.com/compute-product/hip-convert-cuda-to-portable-c-code/</u>





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